1974

THE RECOVERY OF RECORDED DIGITAL INFORMATION IN DRUM, DISK AND TAPE SYSTEMS

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The use of magnetic recording techniques has long been an important means of sorting digital information, as evidenced by the wide variety of equipment currently in use. Representative systems utilize drums, disks and tape as the recording medium.

All three techniques share the common problem of recovering the recorded digital information. The analog signal obtained by passing the recording medium by a magnetic sensor (Read Head) must be converted to a suitable digital format.

This application note reviews the general problem and discusses a number of specific circuit approaches.

***MOTOROLA** Semiconductor Products Inc.*

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GENERAL CONSIDERATIONS

The design parameters of the read circuitry are determined to a large extent by equipment characteristics and recording method. A review of the relevant terminology (expressed in terms of a tape system) will serve to illustrate the relationship. Of particular interest are: tape speed, transfer rate, packing density, and encoding format.

Tape speed, of course, refers to the velocity at which the tape moves past the recording head, and is usually expressed in inches per second (ips). Typical values range from a few ips to several hundred ips, depending on the recording medium.

Transfer rate is simply the specification of how fast data is being handled by the recording system, and is usually expressed in bits per second (or in the case of parallel recording, bytes per second). Packing density refers to the number of bits per inch (bpi) stored on the tape, and it varies from a few hundred bpi to several thousand bpi. Density is determined by the tape speed, data transfer rate, and the physical limitation of the tape. Typical transfer rates are indicated in Table 1.

TABLE 1

System		Transfer Rate
Cassette		2-20 k Bits/S
Cartridge	(a)	50-100 k Bits/S
	(b)	100-500 k Bits/S
Reel	(a)	100-200 k Bits/S
	(b)	200-800 k Bits/S
Disk		1.5-20 M Bits/S

The manner in which a data bit is recorded on the medium also influences the read circuit design. In general, data is written by passing current through an inductive recording head as the tape moves past the head, causing a flux transition to be recorded. The polarity of the flux reversal is determined by the direction of the current through the write head. As the tape is read, each flux reversal is sensed by the read head, and this causes peaks to occur in the read signal.

The specific manner in which a data bit is represented depends on the encoding format being used. There are numerous encoding methods currently in use; however, phase encoding is most widely used and will be used in all examples throughout this report. A typical data block that is to be encoded is shown in row 1 of Figure 1. The phase encoded format records a "one" as a flux transition at the midpoint of the data cell, toward the magnetization level representing erased tape. "Zeros" are recorded as a flux reversal in the opposite direction.
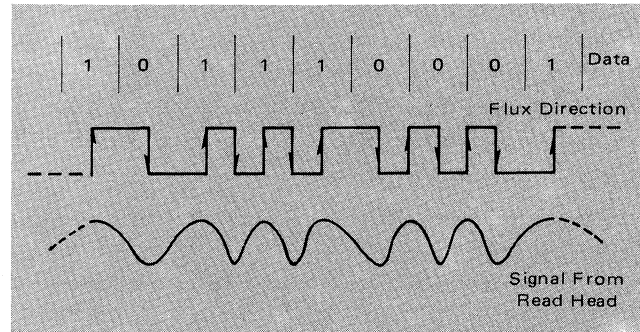

FIGURE 1 — Phase Data Encoded

"Phase transitions" are introduced as needed at the end of each data cell. For instance, if a one is to be recorded immediately following another one, there must be a phase transition so that another transition toward erase polarity can occur at the midpoint of the second data cell. The various possibilities are illustrated in Figure 1. The analog signal resulting from reading such a format is also shown.

READ CIRCUIT DISCUSSION

The first of several approaches to be discussed is shown in Figure 2. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplification", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disk or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels, as well as all other signals referred to in this report, are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB. All references to gain in dB refer to voltage gain, that is:

$$\text{Voltage gain (dB)} = 20 \log_{10} \frac{V_o}{V_{in}}$$

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disk systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733, a video wideband amplifier, has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

The second block shown in Figure 2, peak detection, provides the following stages with precise information as to the polarity and location of all peaks in the amplified signal.
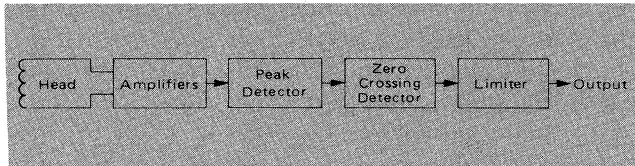

FIGURE 2 – Typical Read Circuit (Approach 1)

There are a number of ways to implement this function and several are shown later in this report. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

The actual circuitry used to differentiate the Read signal varies from a differential LC type in disk systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB (discussed later in this report). Thus, the 2 V signal going into the differentiator is reduced to 200 mV. An example of a typical Read signal with the differentiated output signal is shown in Figure 6, waveshapes a and b.

The next block in Figure 2 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational-amplifier with series or shunt limiting. For higher transfer rates (greater than 100 k B/S) comparators are used. An example of an operational amplifier useful for comparator applications is the MC1709. The MC1709, operated open-loop with no compensation, is considerably faster than compensated counterparts such as the MC1741. Suitable comparators for higher transfer rates are the MC1710, MC1514, MC1711 and MC3302.

MORE COMPLEX APPROACHES

The approach described above is often modified to

include threshold sensing. In Figure 3, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive going peaks and the other for negative going peaks. These comparator outputs are then combined in the output logic gates.
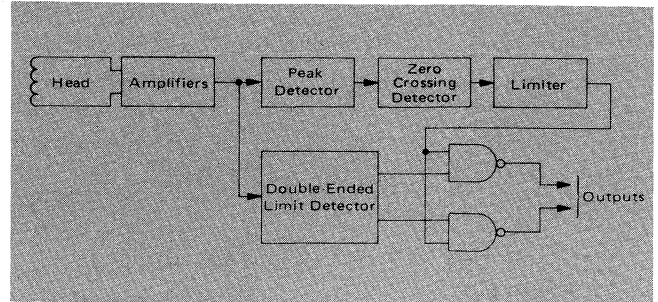

FIGURE 3 – Read Circuit, (Approach 2)

Another common technique is shown in Figure 4. The branch labeled rectifiers, peak detector, etc., provides a clock transition to the D flip-flop that corresponds to the peak to both the positive and negative going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.
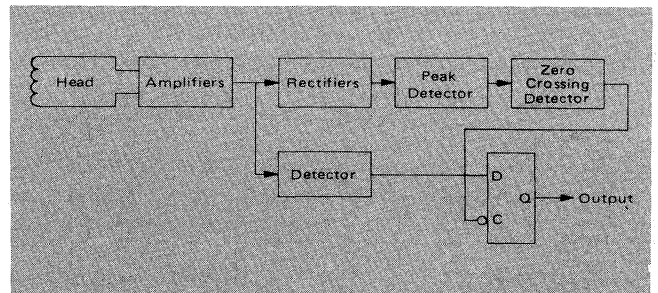

FIGURE 4 – Read Circuit, (Approach 3)

The technique shown in Figure 5 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the approaches shown offer certain intrinsic advantages or disadvantages. The overall decision as to which approach to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Later in the report two design examples are described using approach one and approach four. The basis for choosing approach one was primarily cost (only three integrated circuits were required to implement this ap-

proach). Approach four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.
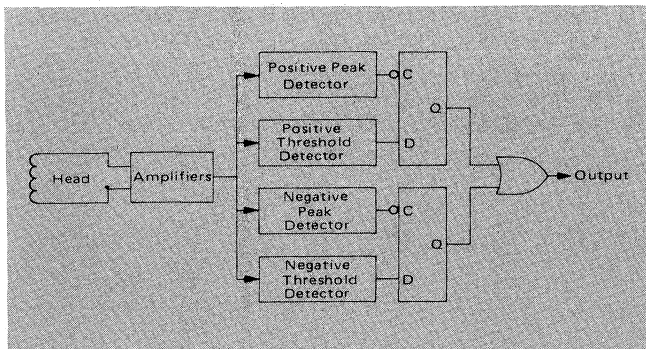

FIGURE 5 — Read Circuit, (Approach 4)

READ CIRCUITS

This section discusses specific circuitry for some of the approaches discussed earlier.

Figure 6, indicates a simple method of implementing the system of Figure 2. As previously discussed, this circuit consists of four sections: the amplifier section, the peak detector, the zero-crossing detector, and the limiter. The example shown in Figure 6 uses a passive circuit, C2R7, for the differentiator and a comparator (MC1710) for the zero-crossing detector and limiter. Amplification is provided by the MC1458 operational amplifier.

Typical waveshapes are included on Figure 6. The second waveshape, the differentiated Read signal, shows the zero-crossing occurring at peaks of the Read signal. The output signal (third waveshape) describes a pulse train when the rising edges correspond to the positive peak of the Read signal and negative edges to negative peaks.

As previously mentioned, the comparator provides the zero-crossing detector and limiter function. There are several ways of implementing this function using operational amplifiers, four of which are shown in Figure 7. In all four, the differentiator is implemented by C1R1.

The second example (Figure 8) describes how approach two (Figure 3) can be implemented. The operation of this circuit is as follows: The first three stages IC1, IC2 and IC3 amplify, differentiate and limit the Read signal in a fashion similar to that shown in Figure 6. The resultant output signal is fed to two AND gates, IC6 and IC7. The output signals from IC6 and IC7 appear only when the gates are enabled by IC4 and IC5. IC4 and IC5 (which are comparators) provide the double-ended limiter function. That is, IC6 and IC7 are enabled only at the positive and negative peaks respectively of the Read signal. The signal magnitude required to trigger the comparator is set by the positive and negative threshold levels.

Typical waveshapes are shown in Figure 9. Note that the leading edge of the pulse train from IC6 corresponds to the positive peaks of the Read signal. The trailing edge of the pulse train from IC7 corresponds to the negative peaks of the Read signals. The output of IC7 drives a "one-shot", IC8. This one-shot triggers on the trailing edge of the
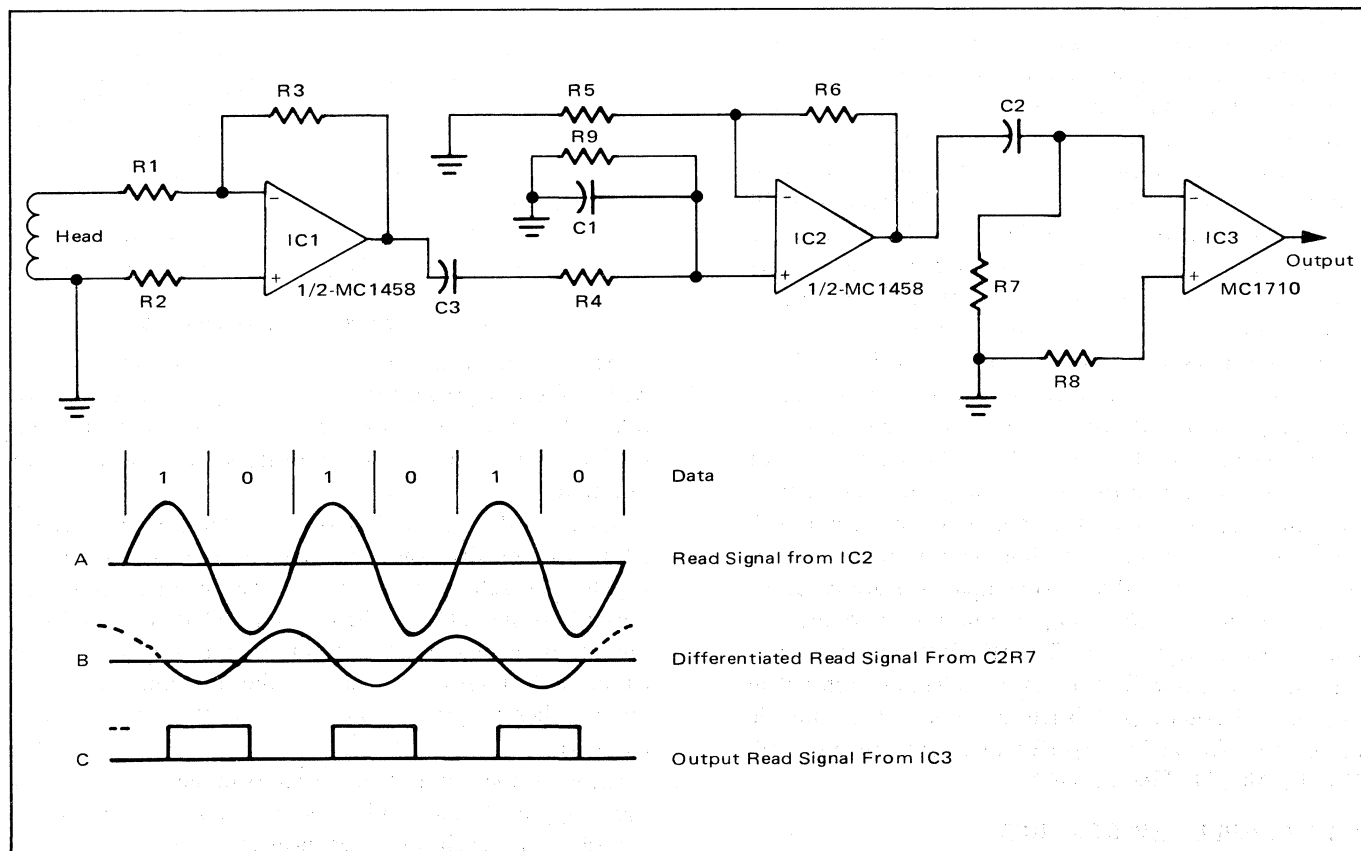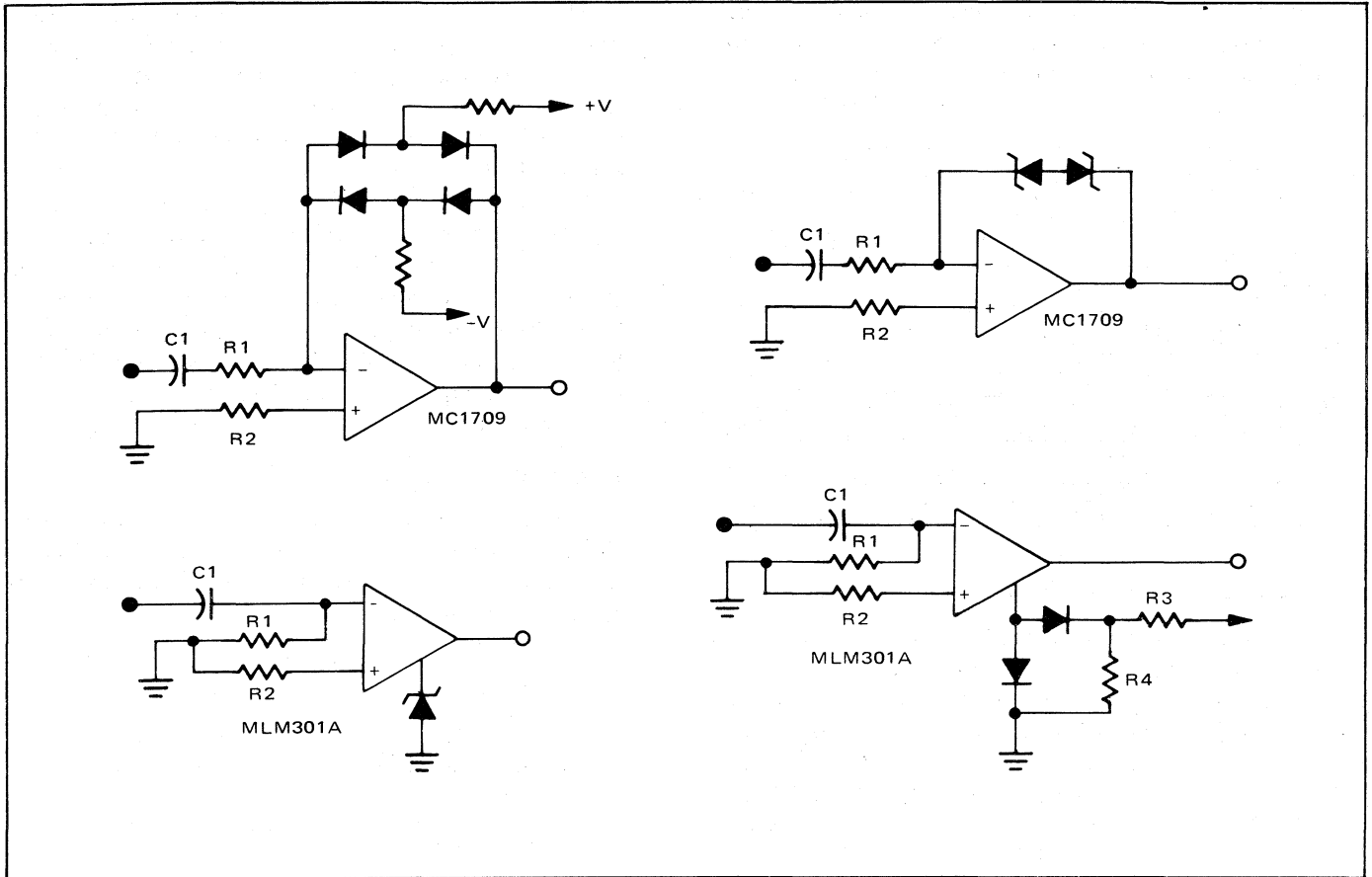

FIGURE 6 — Read Circuit, (Approach 1)

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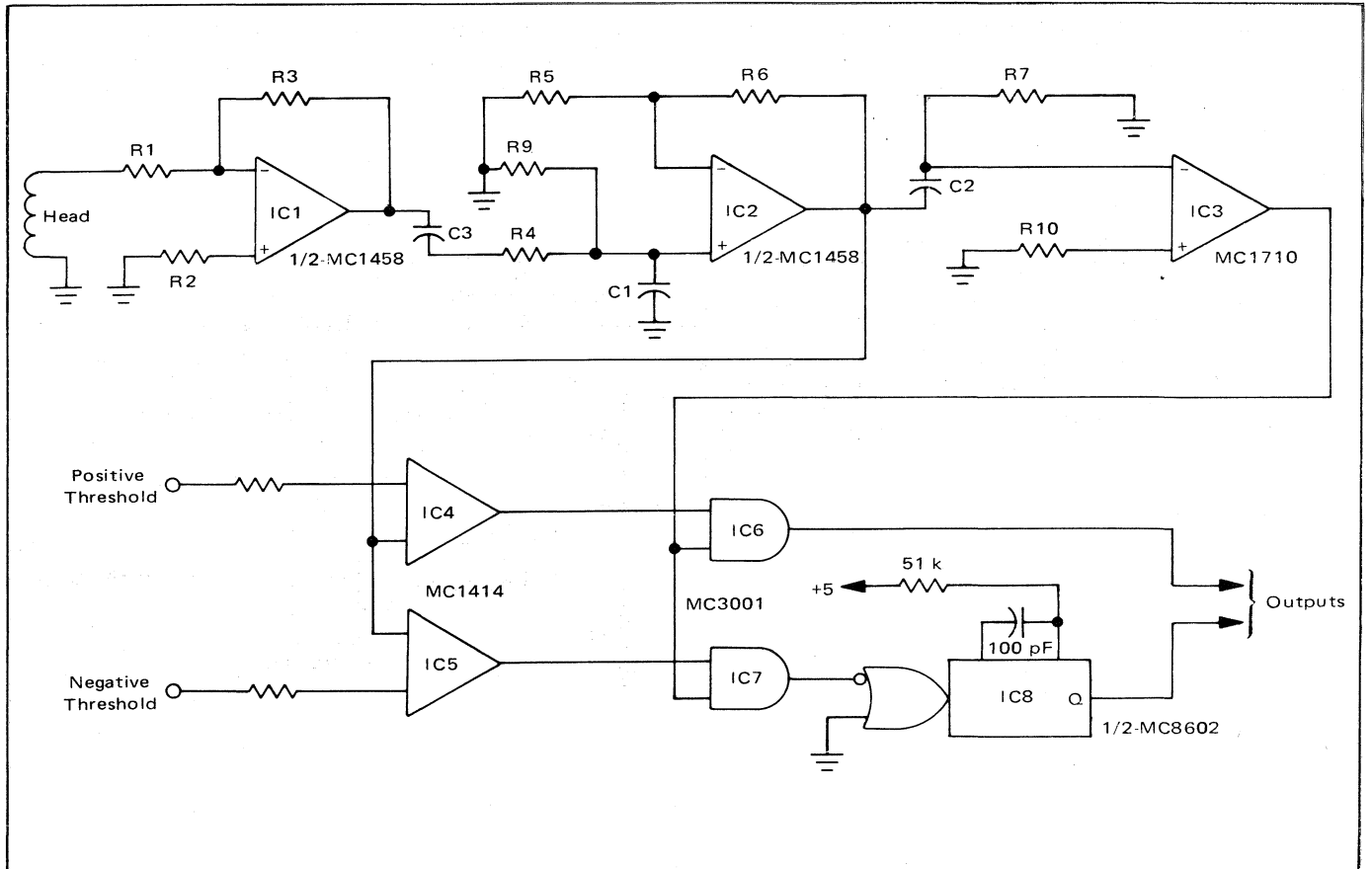
FIGURE 7 — Examples of Using Op-Amps As Limiters

FIGURE 8 — Read Circuit Using Approach 2

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output pulse train from IC7. The desired result, with the leading edge of the signal from IC8 corresponding to negative signal peaks is shown as the last row of Figure 9.
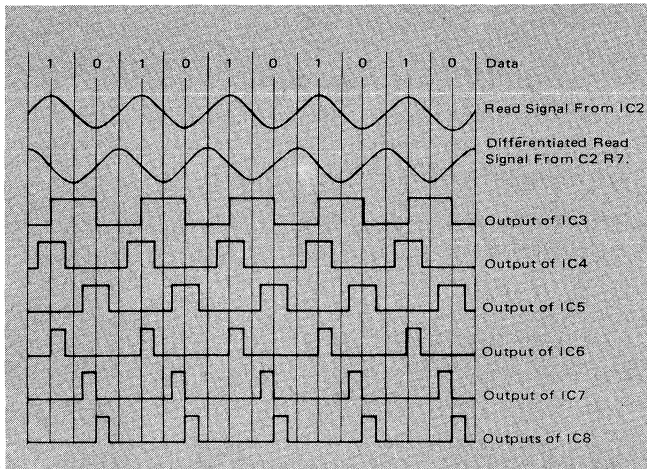

FIGURE 9 — Waveforms for Read Circuit Using Approach 2

The third example (Figure 10) shows how approach three (Figure 4) may be implemented. This circuit works in the following manner: The D flip-flop (IC6) provides an output when clocked by IC4 (1/2-MC1414). IC4 produces a positive going pulse for each positive and negative peak in the Read signal (see Figure 11). IC1 (1/2-MC1458) and IC2 (1/2-MC1458) provide the gain. This amplified Read signal drives D1 directly and D2 indirectly. That is, the signal to D2 is first inverted by IC3, (MC1741), a unity gain amplifier. The resultant rectified Read signal is fed to the differentiator R10C2 and to the zero-crossing detector/limiter IC4 (which is a comparator).

Thus, a pulse train is fed to IC6 with each negative transition corresponding to the positive and negative peaks of the Read signal. In the meantime, the Read signal is fed to IC5, a comparator. When the positive peaks exceed a threshold established by R14, R13 and R15, IC5 supplies a data pulse to IC6.

The fourth example (Figure 12) describes how approach four (Figure 5) may be implemented. Circuit operation is as follows: Positive and negative peaks of the Read signal are processed separately. IC4 and IC3 process the negative going peaks and the positive peaks pass through IC5 and IC6. The outputs of IC4 and IC6 drive T flip-flops, which serve as data inputs to IC7 and IC10. A detailed timing diagram of these waveshapes are provided in Figure 13.

READ CIRCUIT DESIGN

This section describes two design examples of Read circuitry utilizing approaches one and four. Either method is suitable for use in a cassette recorder with the specifications shown in Table 2:

TABLE 2

FRPI*	1600
Tape Speed	15 ips
Head Signal	10 mV at 15 ips
Encoding Method . . .	Phase encoding
Logic	TTL

*Flux reversals per inch with a maximum of two per bit time.

The example using approach one is shown in Figure 14. This circuit approach, as previously explained, uses two stages of gain (MC1458), a passive differentiator to gen-
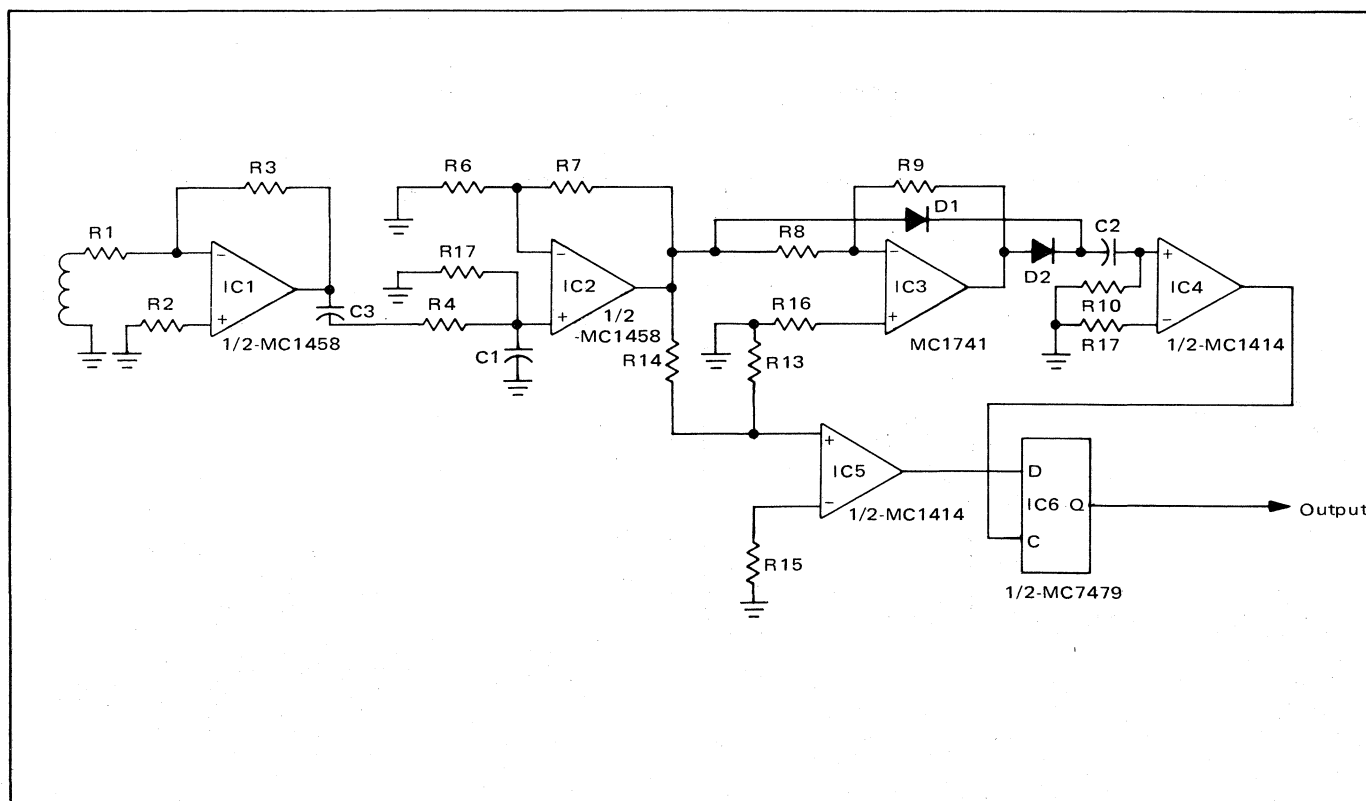

FIGURE 10 — Read Circuit — Approach 3

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erate the zero-crossing, and a comparator as a detector-limiter (MC1710).

The zero-crossing detector and limiter function is implemented using an MC1710 comparator. The minimum signal level to IC3 was chosen to be 70 mV (140 mV peak-to-peak), since signal levels less than 50 mV can cause 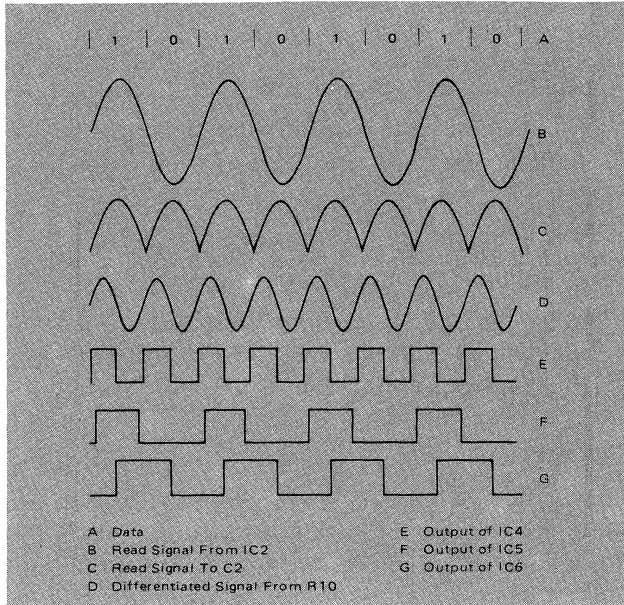undesirable oscillation during the transition period. This is a common problem with comparators. It is usually the result of noise and a slowly changing input waveform, but can be avoided by providing adequate input signal levels. Signal levels less than this will also result in a greater difference between where the zero-crossing points occur and where the MC1710 actually triggers. The resultant error of less than 5 percent was deemed adequate for this design.

The differentiator consists of a simple RC network R7, C2. This network provides the phase shift necessary to generate the zero-crossing at both positive and negative peaks of the Read signal. In addition to providing phase shift, this network also attenuates the signal. Figure 15, shows the phase shift and attenuation as a function of normalized frequency for this type of differentiator. From this figure note that a value of $F = 0.07\ f_c$ results in a phase shift and attenuation of 86 degrees and 23 dB respectively. This difference of 4 degrees from the desired 90 degrees will result in an error of less than 5 percent in regard to actual peak location.

For a value of $0.07\ f_c$ and a minimum frequency f_{min} the corner frequency, f_c is:

$$f_c = \frac{f_{min}}{0.07}$$

The minimum frequency corresponds to one-half the value of f_{max}. This frequency (f_{min}) occurs when alternate "1's" and "0's" are recorded, and no phase transitions are

FIGURE 11 — Waveforms for Read Circuit Using Approach Three

A Data
B Read Signal From IC2
C Read Signal To C2
D Differentiated Signal From R10
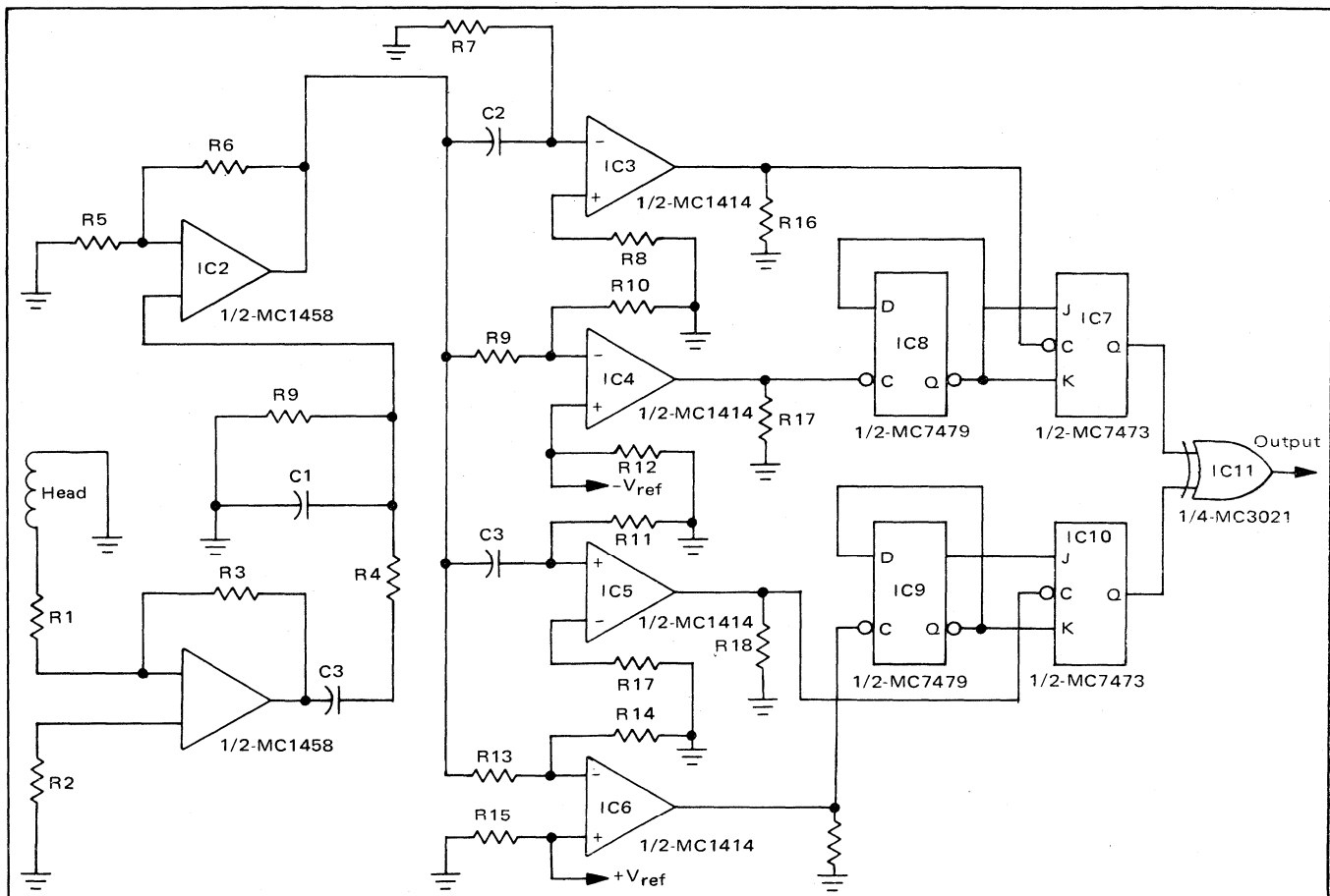E Output of IC4
F Output of IC5
G Output of IC6

FIGURE 12 — Read Circuit Using Approach 4

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required at the end of the data cells. The maximum frequency can be calculated from tape speed, and the maximum flux reversals per inch as:

$$f_{max} = \frac{1600\text{-flux reversals}}{\text{inch}} \times \frac{15\text{-inches}}{\text{sec}} \times \frac{\text{cycle}}{2\text{-flux reversals}}$$

of 12 kHz.

Correspondingly,

$$f_{min} = \frac{f_{max}}{2}$$
$$= 6 \text{ kHz}$$

Thus, as explained earlier, the corner frequency providing less than 5% phase error is:

$$f_c = \frac{6 \text{ kHz}}{0.07}$$

or 86 kHz

Choosing a value of R7, much less than the parallel input resistance of the comparator, will assure that the corner frequency is determined by C2R7 only. With this consideration in mind, R7 was chosen to be 91 ohms. C2 was then calculated to be 0.1 μF.

The 23 dB of attenuation, in conjunction with the desired level of 140 mV (peak-to-peak) into IC3, necessitates a minimum drive level to the differentiator of 2000 mV at 6 kHz. At 12 kHz the attenuation is 17 dB for the given values of R7 and C2. Thus, the minimum drive level to the differentiator at 12 kHz is 1000 mV.

The final step in the design is determining the Read amplifier requirements. It involves considerations such as, how much gain is required, what is the bandwidth requirement, and how much outband roll-off is required.

The overall gain requirement is straightforward in that the 10 mV signal available from the Read head must be amplified to the previously determined level of 2000 mV (at 6 kHz) to drive the differentiator. This overall gain is:

$$A = 20 \log_{10} \frac{2000 \text{ mV}}{10 \text{ mV}}$$
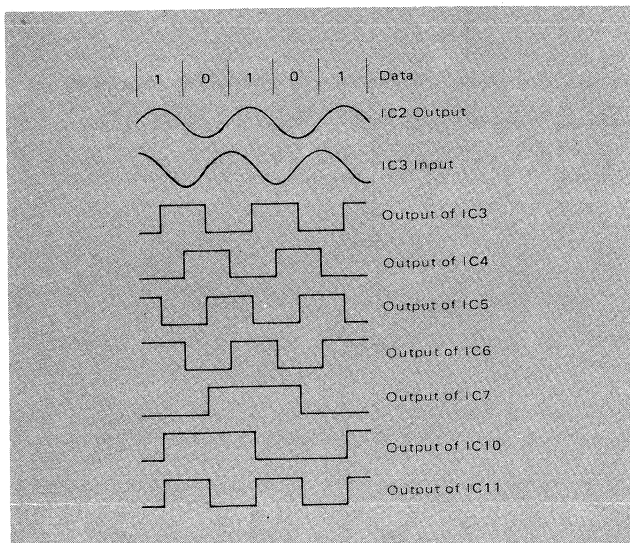
or 46 dB

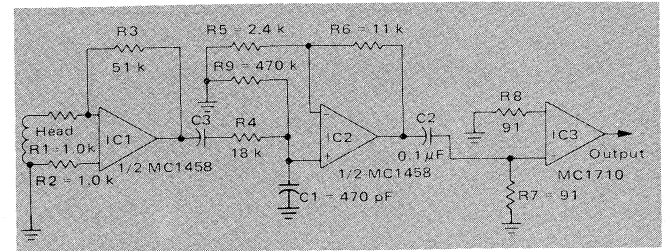**FIGURE 13 – Waveforms For Read Circuit Using Approach 4**

FIGURE 14 – Read Circuit, Design Example 1

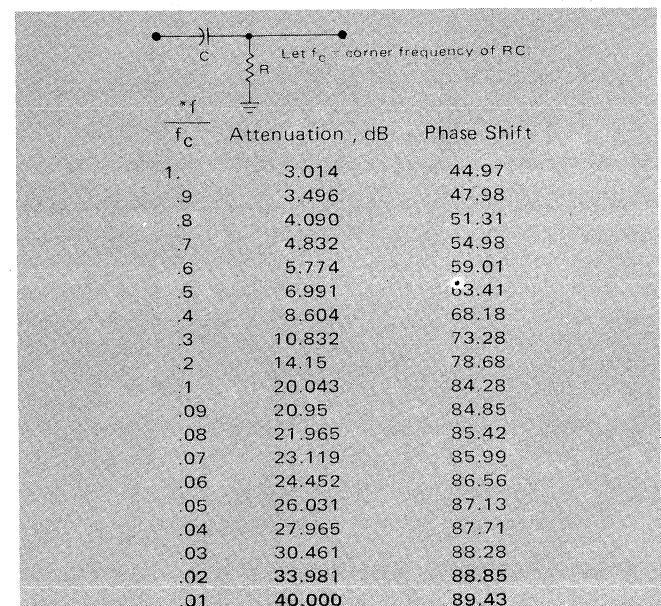Correspondingly, the required gain at 12 kHz is 40 dB.

The required bandwidth, based on the maximum frequency of interest was previously determined to be 12 kHz.

The outband response is more involved, and includes among other things the response of the differentiator. The differentiator, used in this example, is actually a high-pass filter which readily passes noise* higher than 12 kHz (6 dB per octave). Therefore, it is highly desirable to incorporate at least 6 dB per octave of outband roll-off in the Read amplifier. The actual filter used in practice varies with system and manufacturer. For instance, it is not uncommon to see Read amplifiers with 18 dB per octave of outband roll-off in a reel tape system.

This design provides 12 dB per octave of outband roll-off using the normal 6 dB per octave of the first IC (with the corner frequency properly chosen), and the 6 dB per octave roll-off of a simple RC low-pass filter. Both corner frequencies should be at 19 kHz to achieve an overall 3 dB bandwidth of 12 kHz. Placing the corner frequency of the first IC (1/2-MC1458) at 19 kHz results in a closed loop gain of 32.5 dB at 12 kHz. The value of R3 for R1 equal to 1000 ohms is approximately 52 k ohms from:

$$A = \frac{R3}{R1}$$

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*That is, noise figure is increasing directly as the attenuation. The severity of this problem depends on the signal level going into the differentiator and the filter characteristics.

$\frac{*f}{f_c}$	Attenuation, dB	Phase Shift
1.	3.014	44.97
.9	3.496	47.98
.8	4.090	51.31
.7	4.832	54.98
.6	5.774	59.01
.5	6.991	63.41
.4	8.604	68.18
.3	10.832	73.28
.2	14.15	78.68
.1	20.043	84.28
.09	20.95	84.85
.08	21.965	85.42
.07	23.119	85.99
.06	24.452	86.56
.05	26.031	87.13
.04	27.965	87.71
.03	30.461	88.28
.02	33.981	88.85
.01	40.000	89.43

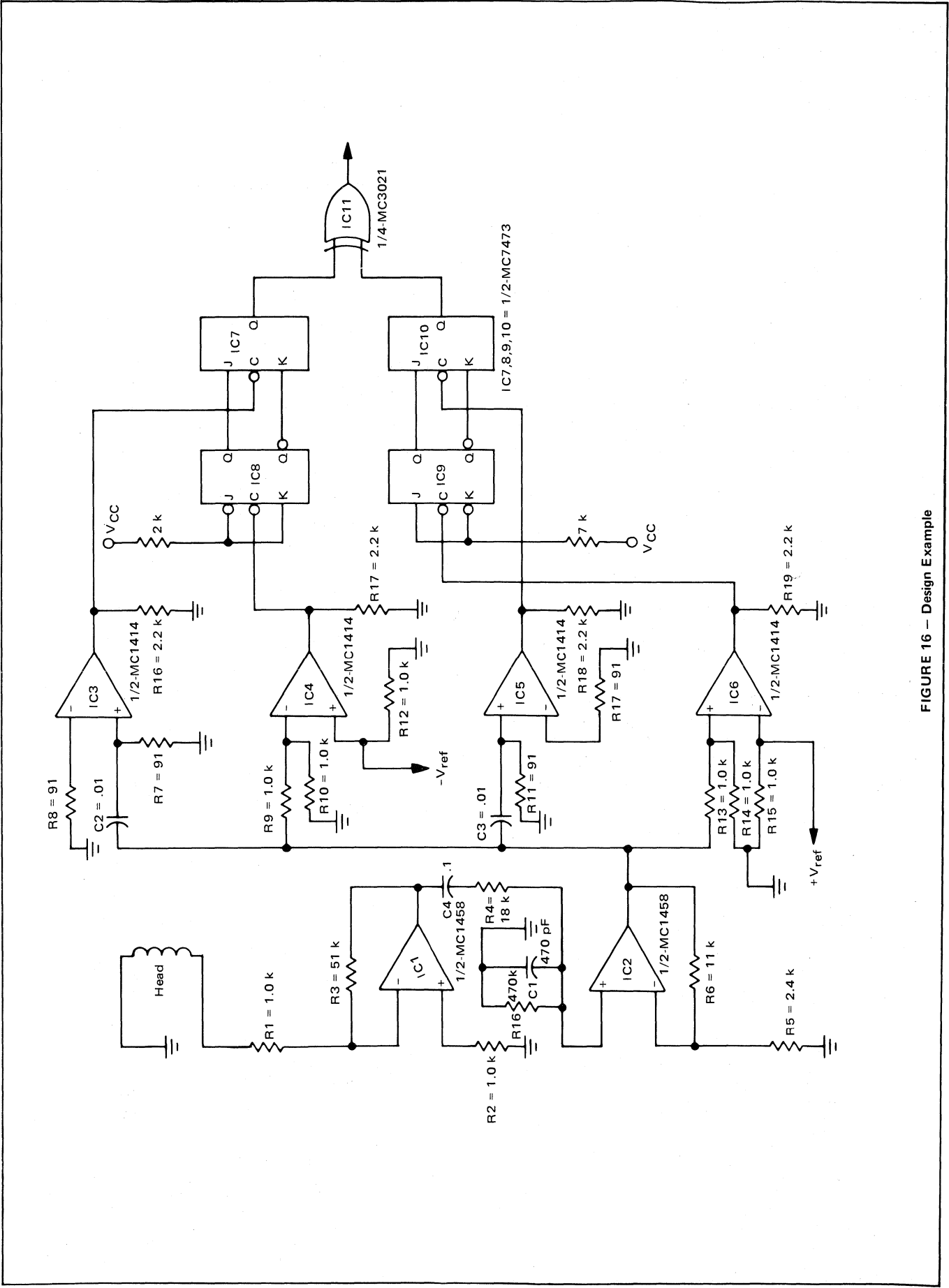*Where f_c is the –3.0 dB corner frequency
FIGURE 15

FIGURE 16 — Design Example

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where A = 34 dB (which is the gain if there were no roll-off at 12 kHz).

The second network R4, C1 is also selected to have a corner frequency of 19 kHz. Choosing a convenient value of C1 equal to 470 pF results in a value of 18 k ohms for R4.

As previously discussed, the overall gain of the Read amplifier (IC1 and IC2) must be 46 dB at 6 kHz and 40 dB at 12 kHz. The first stage gain was determined to be 34 dB, excluding the 1.5 dB roll-off at 12 kHz. To insure that adequate overall gain is available, the second stage is designed for 6 kHz, rather than 12 kHz. The gain of the second stage must be sufficient to provide the difference between the total required gain (46 dB), the first stage gain 34 dB, and the roll-off. The roll-off of either IC1 or the low pass filter is approximately 0.5 dB at 6 kHz. Thus, the required gain of the second stage is 46 dB + 1 dB -34 dB, or 13 dB. A closed loop gain of 13 dB using (1/2-MC1414) results in a bandwidth of approximately 150 kHz. From the expression for gain in a non-inverting amplifier:

$$A = 1 + \frac{R5}{R4}$$

For R5 = 11 k, R4 equals approximately 3.3 k. Using this design, the overall gain of the read amplifier at 12 kHz is 34 dB + 13 dB − 3 dB, or 44 dB. This value is 4 dB higher than the minimum required value of 40 dB.

The Read amplifier for the components calculated has an overall gain of 46 dB at 6 kHz, 44 dB at 12 kHz, a 3 dB bandwidth of 12 kHz and an outband roll-off of 12 dB per octave.

The second design example is shown in Figure 16. As previously discussed, this design uses approach 4. With the exception of IC7 through IC11 and IC4 and IC6, the design is the same as Figure 14. For instance, although two differentiators (C2, R7 and C3R11) are used the corner frequency for each is again 86 kHz. Also the required signal level to IC3 and IC5 is approximately 70 mV. The Read amplifier design is also identical to Figure 14.

The threshold circuitry IC4 and IC6 is unique to this design. The threshold of either IC can be varied by changing $+V_{ref}$ and $-V_{ref}$. For instance, increasing $+V_{ref}$ will require a large signal to the non-inverting terminal of IC6 — thus providing a higher degree of noise immunity. Typical values of V_{ref} (both positive and negative) were experimentally determined to be approximately 1 volt for the cassette system evaluated.

SUMMARY

The general problem of recovering digital information stored on a recording medium such as drum, disk and tape is discussed. General circuit approaches, as well as specific circuit examples are shown. Two design examples of Read Circuitry design are included.

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